

Student name: _____ Section 4(9.05) or 3(12.20)

Midterm Exam - II for CSE 271 Sections (3) and (4) Fall 2005

11/9/2005 - 8:15-10:15 p.m. - 112 Kern

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Answer all questions in the space provided Use back page if more space needed.

(Total 60 points)

1. Use K-map method to design and draw a minimum two level circuit corresponding to the sum of products expressions using AND gates and one OR Gate per function for the following two output functions. (10 points)

$$f(a, b, c, d) = \sum m(0, 1, 2, 3, 5, 7, 8, 10, 11, 13)$$

$$g(a, b, c, d) = \sum m(0, 2, 5, 8, 10, 11, 13, 15)$$

2. Use Quine –McCluskey method find all PIs of the incompletely specified function $F(W, X, Y, Z) = \sum m(1, 3, 4, 6, 11) + \sum d(0, 8, 10, 12, 13)$. Next use the tabular method to minimize the function, design and draw the minimal cost SOP form of the 2-level circuit using only AND and OR gates. (10 points)

3. For the following set of functions:

$$B(a, b, c, d) = \sum m(2, 3, 5, 7, 8, 10, 13) + \sum d(0, 1, 14, 15)$$

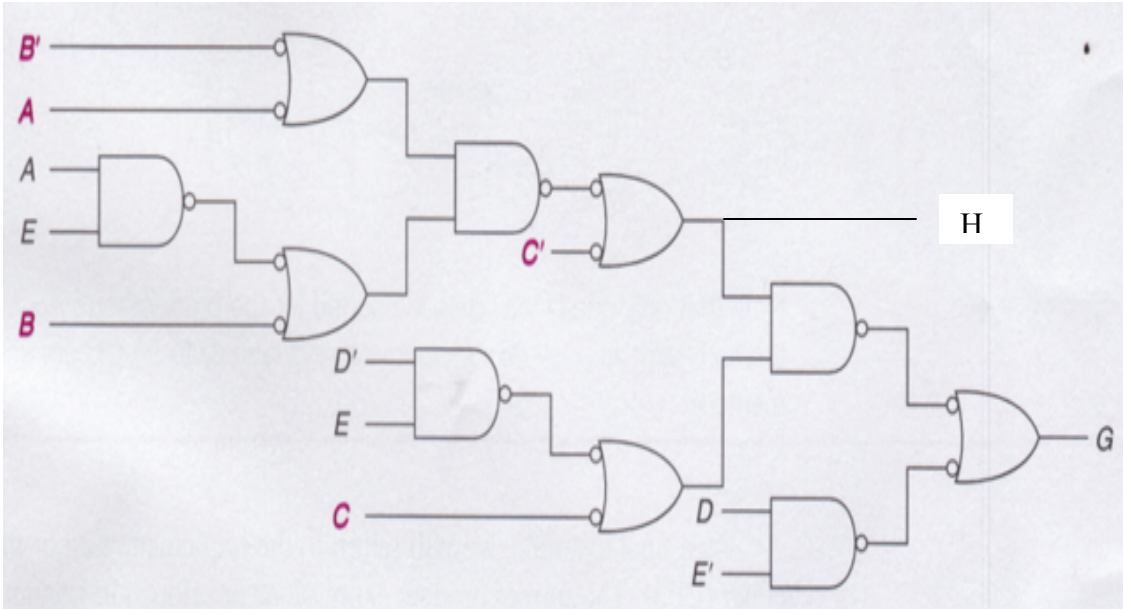
$$K(a, b, c, d) = \sum m(2, 3, 4, 6, 7) + \sum d(0, 1, 14, 15)$$

The possible shared terms are given to be abc , $a'b'$, $a'cd$, bcd , other prime implicants (PI)

of $K(a, b, c, d)$ are $a'c$, bc , $a'd'$ and other PIs of $B(a, b, c, d)$ are: $a'd$, bd , acd' , $b'd'$.

Find a set of minimum sum of products expressions corresponding to a two-level AND/OR gate (7 points) and draw the circuit diagram. (3 points)

4. Write the functions H and G realized by the above circuit (4 points). Give the delay from B to H and compute the maximum delay in the circuit assuming T is the delay at each gate and all inputs are available both uncomplemented and complemented. (4 points)
 Define a glitch and how is it related to gate delays? (2points)



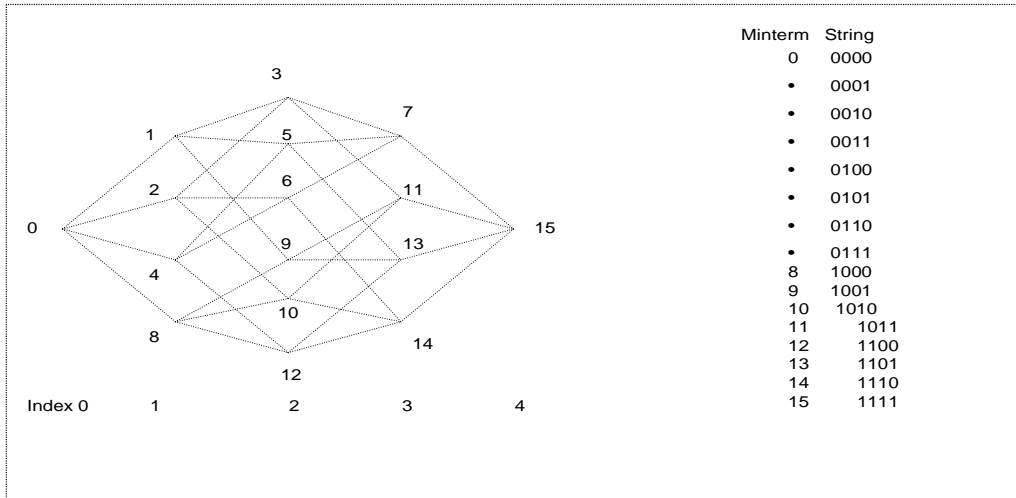
5. For an active high output decoder with two inputs and an active low enable input provide the following. (10 points)

- a. The truth table
- b. A circuit diagram consisting of AND and NOT gates

6. (a.) A, B, C and D are the input data, S1 and S0 denote the “Select” inputs of a 4-way multiplexer with 4 AND gates, one OR gate and 2 not gates. Draw the circuit diagram of the multiplexor(4 points).
- b. Provide the connection diagram for realizing the 4 – way multiplexer using two 2-way multiplexers (3 points)
- c. Write the truth table for a three-state buffer and draw a diagram of a 2-way multiplexer that uses two three-state gates (3 points)

Extra credit problem (4 point bonus). Use the graph theoretic (not the K-map) approach to determine MSOP for the Question 1 and verify the solution that you obtained already. You may use the following 4- cube structure to find the terms, EPIs , PIs etc.

The 4-cube (n = 4)

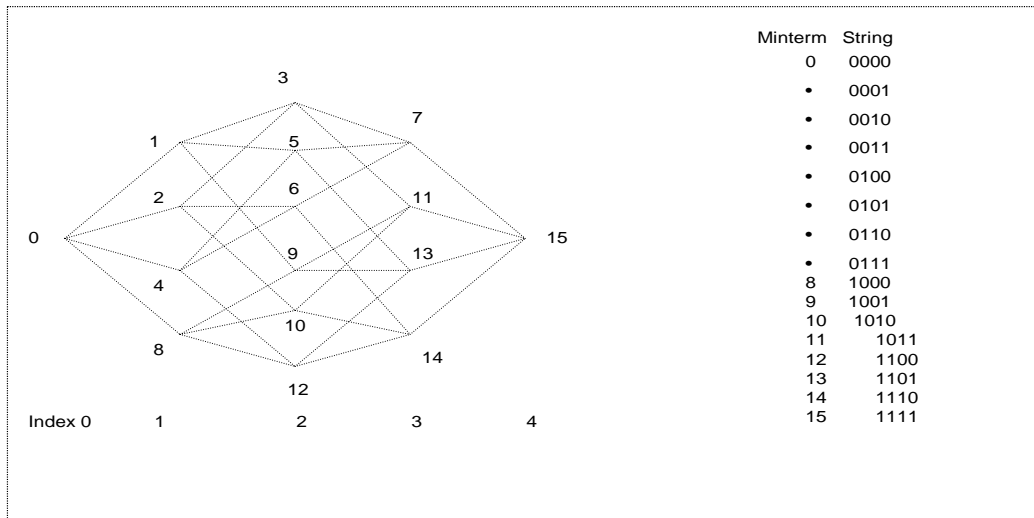


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KVB(16+) - 2

The 4-cube (n = 4)



10/17/05

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KVB(16+) - 2

Student Name _____ Section 3(12.20) or 4 (9.05AM)

**Take home part of the Midterm exam II, CSE271. Answer both questions
(15 points each question).**

**Complete and submit at the entry to exam hall before taking your exam. Attach
additional paper as needed to this answer sheet**

1. Using Quine Mcklusky method determine all of the a minimum cost solutions for the function $h(p,q,r,s) = \sum m(0,2,5,8,10,14)$. Show all the steps.

Draw one of the the minimum cost circuit diagram. (15 points)

2. Do Question 17 page 351 and 352 of your text. Show all steps (15 points).

(Bonus 3pt) Find all the MSOP solutions for the function $q(r,s,t,u) = \sum m(1,2,4,8)$ and draw the MSOP circuit diagram(s)